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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,710	12/05/2003	Yakov Belopolsky	FCI-2731/C3274A	4213

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EXAMINER
BUI, HUNG S

ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/729,710	BELOPOLSKY, YAKOV	
	Examiner	Art Unit	
	Hung S. Bui	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/16/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/16/2007 has been entered.

Oath/Declaration

2. The oath/declaration filed on 12/05/2003 is acceptable.

Information Disclosure Statement

3. The IDS filed on 10/16/2007 have been considered and made of record.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 4 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dozier, II et al. [US 5,772,451] in view of Noschese [US 4,767,344] and Findeis et al. [US 6,203,690].

Regarding claims 1 and 4, Dozier, II et al. disclose an electronic assembly, comprising a printed circuit board substrate (302, figure 3, column 22, line 23) including a retentive through hole (352, figures 3, column 26, line 11), a plurality of lands (306, figure 3), and an electrical connector (300, figure 3, column 23, lines 50-52), the electronic connector comprising:

- a housing (300, figure 3);
- a plurality of solder masses (314, figure 3, column 26, line 24) extending from a surface of the housing for electrically connecting the electrical connector to the land of the circuit substrate (figure 3); and
- a retention structure (350, figure 3, column 26, line 11) extending from the surface of the housing spaced apart from the plurality of solder masses (figure 3) and positioned within the thorough holes; and
- the retention structure having a cross-sectional area smaller than an area of the through hole so that a clearance exists between the retentive structure and a periphery of the through hole (figure 3).

Dozier, II et al. disclose the instant claimed invention except for the retentive structure is made with a base material and a plating material disposed over at least a portion of the base material; and wherein at least some of the plating material separates from the base material at a reflow temperature of the plurality of solder masses and combines with a solder composition within the through hole so that the solder composition and the plating material, upon cooling, form a bond between the printed circuit substrate and the retentive structure.

Findeis et al. disclose a chip carrier (10, figures 1-3) having at least one retentive element (16) being mounted thereon, wherein the retentive element comprises a base material (Nickel layer 22) and a plating material (Gold layer 24) covered the base material (figures 1-3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the retentive element design of Findeis et al. for the retentive structure of Dozier, II et al., for the purpose of providing thermal conductivity between the socket/housing and the circuit board.

Noschese discloses an electronic assembly (figures 3-4) having a housing (22, figure 3, column 4, line 23); a circuit substrate (32, figure 3, column 4, line 49) including a retentive through hole (a through hole including a copper plating 46 as shown in figures 3-4), at least one retentive structure (26, figures 3-4, column 4, line 13) extending from the surface of the housing, and the retentive through hole is filled with a solder composition material (column 4, lines 56-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the retentive structure design of Noschese in Dozier, II et al., as modified, for the purpose of permanently mounting the housing socket onto the circuit substrate.

Regarding claim 2, Dozier, II et al., as modified, disclose wherein the reflow temperature is about 90 or 180 degrees.

Regarding claim 6-7, Dozier, II et al., as modified, disclose the instant claimed invention except for the specific volume percentage of material associated with the solder.

The specific volume percentage of material associated with the solder would have been an obvious design consideration based on the specific fabrication technique used to mount the electrical component.

6. Claims 8-11 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dozier, II et al. [US 5,772,451] in view of Noschese [US 4,767,344].

Regarding claims 8-9, Dozier, II et al. disclose an electronic assembly, comprising a printed circuit board substrate (302, figure 3, column 22, line 23) including a retentive through hole (352, figures 3, column 26, line 11), a plurality of lands (306, figure 3), and an electrical connector (300, figure 3, column 23, lines 50-52), the electronic connector comprising:

- a housing (300, figure 3);
- a plurality of solder masses (314, figure 3, column 26, line 24) extending from a surface of the housing for electrically connecting the electrical connector to the land of the circuit substrate (figure 3); and
- a retention structure (350, figure 3, column 26, line 11) extending from the surface of the housing spaced apart from the plurality of solder masses (figure 3) and positioned within the thorough holes; and

- the retention structure having a cross-sectional area smaller than an area of the through hole so that a clearance exists between the retentive structure and a periphery of the through hole (figure 3).

Dozier, II et al. disclose the instant claimed invention except for the retention structure made with a material that combines with a solder composition within the through hole and enables continued affixation of the electrical connector to a circuit substrate at temperatures sufficient to initiate reflow of the plurality of solder masses.

Noschese discloses an electronic assembly (figures 3-4) having a housing (22, figure 3, column 4, line 23); a circuit substrate (32, figure 3, column 4, line 49) including a retentive through hole (a through hole including a copper plating 46 as shown in figures 3-4), at least one retentive structure (26, figures 3-4, column 4, line 13) extending from the surface of the housing, and the retentive through hole is filled with a solder composition material (column 4, lines 56-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the retentive structure design of Noschese in Dozier II, et al., for the purpose of permanently mounting the housing socket onto the circuit substrate.

Regarding claim 10-11, Dozier, II et al., as modified, disclose wherein the reflow temperature is various degrees.

Regarding claim 16, Dozier, II et al., as modified, disclose a plurality of solder masses (314, figure 3) extending from a surface of the housing for electrically connection to a circuit substrate (302, figure 3).

Regarding claim 17, Dozier, II et al. disclose an electronic assembly, comprising a printed circuit board substrate (302, figure 3, column 22, line 23) including a retentive through hole (352, figures 3, column 26, line 11), a plurality of lands (306, figure 3), and an electrical connector (300, figure 3, column 23, lines 50-52), the electronic connector comprising:

- a housing (300, figure 3);
- a plurality of solder masses (314, figure 3, column 26, line 24) extending from a surface of the housing for electrically connecting the electrical connector to the land of the circuit substrate (figure 3); and
- a retention structure (350, figure 3, column 26, line 11) extending from the surface of the housing spaced apart from the plurality of solder masses (figure 3) and positioned within the thorough holes; and

Dozier, II et al. disclose the instant claimed invention except for the retention structure comprising a material that combines with a solder composition within the through hole and after initial affixation of the solder masses with the circuit substrate, affixation at the solder masses is compromised, due to an elevated temperature, prior to affixation at the retentive structure.

Noschese discloses an electrical connector (figures 3-4) having a housing (22, figure 3, column 4, line 23); a circuit substrate (32, figure 3, column 4, line 49) including a retentive through hole (a through hole including a copper plating 46 as shown in figures 3-4), at least one retentive structure (26, figures 3-4, column 4, line 13) extending from the surface of the housing, wherein the retentive structure is positioned

in the retentive through hole and filled with a solder composition material (column 4, lines 56-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the retentive structure design of Noschese in Dozier, II et al., for the purpose of permanently mounting the housing socket onto the circuit substrate.

7. Claims 3, 5 and 13, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dozier, II et al., as modified, as applied to claims 1 and 9 above, and further in view of Melton et al. [US 5,086,966].

Regarding claims 3, 5, 13 and 15, Dozier, II et al., as modified, disclose the instant claimed invention except for the plating material/join being formed of palladinum.

Melton et al. disclose the use of palladinum in a solder composition for mounting an electrical component (column 1, line 65 – column 2, line 14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use gold/palladinum with the solder composition of Dozier, II et al., in view of Noschese and Findeis et al., as suggested by Melton et al., the purpose of improving solder wetting.

8. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dozier, II et al., as modified, as applied to claim 9 above, and further in view of Findeis et al. [US 6,203,690].

Regarding claims 12 and 14, Dozier, II et al., as modified, disclose the instant claimed invention except for the retentive structure is made with a base material and a plating material disposed over at least a portion of the base material.

Findeis et al. disclose a chip carrier (10, figures 1-3) having at least one retentive element (16) being mounted thereon, wherein the retentive element comprises a base material (Nickel layer 22) and a plating material (Gold layer 24) covered the base material (figures 1-3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the retentive element design of Findeis et al. for the retentive structure of Dozier, II et al., as modified, for the purpose of providing thermal conductivity between the socket/housing and the circuit board.

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dozier, II et al., as modified, as applied to claim 1 above, and further in view of Zeng et al. [US 6,434,016].

10. ***Regarding claim 19***, Dozier, II et al., as modified, disclose the instant claimed invention except for an additional electronic connector being mounted another side of the circuit substrate.

Zeng et al. disclose a printed circuit board (200, figure 2a) having at least one electronic component (205, figure 2a) being mounted on a first side thereon, and at least a second component (220, figure 2a) being mounted on a second side of the printed circuit board.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to mount an additional electronic connector on another side of the circuit substrate of Dozier, II et al., as modified, as suggested by Zeng et al., for the purpose of providing additional socket can be used within the circuit substrate.

Response to Arguments

11. Applicant's arguments with respect to claims 1-17 and 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung S. Bui whose telephone number is (571) 272-2102. The examiner can normally be reached on Monday-Friday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gutierrez F. Diego can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

01/05/2008
Hung Bui
Art Unit 2841